Bottom-gated Epitaxial Graphene on SiC (0001)

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We carry out experiments employing epitaxial graphene, fabricated by thermal decomposition on 6H SiC (0001) surfaces [1,2]. A major advantage of this material is the reproducible fabrication of large area and high-quality graphene on an insulating surface. This allows, for example for building graphene Hall bars on atomically flat substrate terraces. However, a disadvantage was so far the absence of a back gate, because the graphene is grown out of the substrate material and an intermediate insulating oxide layer is not possible.

Here we present the controlled fabrication of a bottom gate in the SiC with standard semiconductor technology [3]. A conductive layer at d = 700nm below the surface acts as gate electrode. It is created via implantation of nitrogen ions prior to the graphene growth. It is contacted to the surface with a box-like implantation of a high dose (16 different energies between 30keV and 2MeV). Hence, we define insulating layers and conducting layers by controlling the dopands. The setup is shown in Fig. 1.

A conversion of the graphene layer to quasi-freestanding epitaxial graphene turned out to be mandatory for a working device. This material is hole-filled in contrast to the electron filled standard epitaxial graphene and in magnetotransport measurements it shows the pseudo-relativistic behavior unique for graphene.

A gate voltage applied to the implanted layer enables a variation of the charge carrier density over a wide range. We, find two different regimes of gating mechanisms with strongly different gating efficiency. First for low implanted doses or low temperatures the SiC between gate electrode and surface is insulating and the device behaves like an implanted plate capacitor (IPC). Second we find a Schottky capacitor (SC) regime for high implantation doses or high temperatures. Here the SiC gains a finite conductivity and the capacitance is mainly governed by the Schottky contact between SiC and graphene. The capacitance is higher by a factor of four compared to the IPC regime and is no longer independent from the gate voltage. With this extended Schottky model we can simulate the temperature dependence of the capacitance in Fig. 2. Illumination with ultra violet light extends the SC regime to lower temperatures by generating free carriers in the SiC.

References

[1] Emtsev et val. Nature materials 8, 203 (2009).
[2] Jobst et al. Phys. Rev. B. 81, 195434 (2010)
[3] Submitted to Nature materials

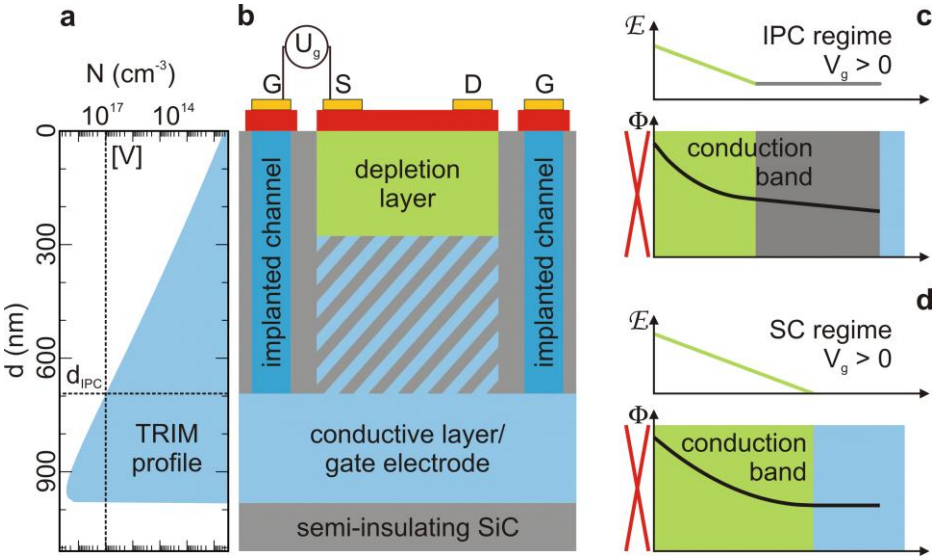

***Fig. 1 a**, TRIM simulation of the implantation profile. The SiC is conducting where the implanted dose exceeds the vanadium compensation [V] (dotted line) and insulating elsewhere. **b**, Setup of the bottom gate with source (S), drain (D) and gate (G) electrodes on graphene; conductive gate layer and implanted connections. In the IPC regime the shaded area is insulating, in the SC regime conducting **c**, Electric field and band diagram for the region between graphene and implanted electrode in the IPC regime, which is self-consistently calculated in our extended Schottky model. A constant external electric field is superimposed onto the built-in field of the depletion layer. **d**, Electric field and band diagram for the SC regime. The conductive layer extends up to the depletion layer. Hence, the whole applied voltage drops across the depletion layer.*

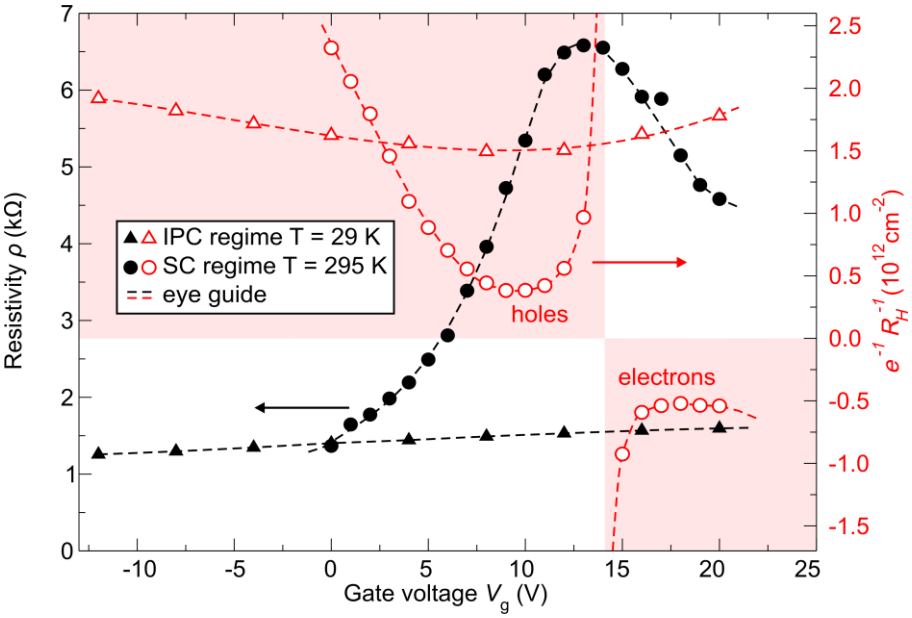

***Fig. 2** Gate response of ρ and $1/eR_H$ of sample HD3 in the IPC (triangles) and the SC regime (circles). The capacitance is much higher in the SC than in the IPC regime. In addition the minimal measured charge carrier concentration $n_{min} = (1/eR_H)_{min}$ is much smaller in the SC than in the IPC regime indicating a higher homogeneity.*